MULTIMEDIA UNIVERSITY®

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2016/2017

EEE1036 DIGITAL LOGIC DESIGN

(All Sections / Groups)

30 MAY 2017
2:30 P.M – 4:30 P.M.
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This question paper consists of 8 pages including the cover page with 4 questions only.

2. Attempt all four questions. All questions carry equal marks and the distribution of marks is given in the questions.

3. Please print all your answers in the answer booklet provided.

4. State all assumptions clearly.

Question 1 (25 marks)

(a) Draw a diagram to show the various components of a general digital computer. Indicate how the data and control signals flow in this diagram.

[6 marks]

(b) Name and differentiate the two major types of digital logic design.

[4 marks]

(c) Fill up Table Q1 which shows 2 numbers (one per row) in different bases. Reproduce the table in the answer booklet. Steps are not required.

[8 Marks]

Table Q1

Binary	Octal	Decimal	Hexadecimal
	244.34		A4.7
110111010.101		442.625	

(d) Perform the following operations in 2's complement system. Use 8 bits (including the sign bit) for each number. Show the steps. Comment on the **correctness** of the results.

(i) $-67 - 34$

[2 Marks]

(ii) $75 + 54$

[2 Marks]

(e) Perform the following operations:

(i) BCD addition for 71 and 89. Show the steps.

[2 Marks]

(ii) Convert binary number 10011101 to Gray code. Steps are not required.

[1 Mark]

Continued ...

Question 2 (25 marks)

(a) Simplify the Boolean expression below using **Boolean algebra**. Show each simplification step clearly.

$$ABCD + (\overline{AB})CD + AB(\overline{CD})$$

[5 marks]

(b) Develop a **truth table** for the expression below:

$$\overline{A}B + \overline{A}\overline{C} + AB\overline{C} + A\overline{B}C$$

[5 marks]

(c) With the aid of Karnaught maps, find the sum-of-product (SOP) **prime implicants** and **essential prime implicants** for the following Boolean function. Hence, find the **minimum SOP** expression of the Boolean function. Show the worked Karnaugh maps.

$$F(A,B,C,D) = \Sigma(0,2,3,5,7,8,9,10,11,13,15).$$

[8 marks]

(d) For the truth table in Table Q2, find the minimum **product-of-sum** (POS) logic expression of output Y using Karnaugh map.

[7 marks]

Table Q2

Inputs				Output
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Continued ...

Question 3 (25 marks)

(a) Draw the timing diagram of the **clock (CLK), Q_0 and Q_1** of the counter shown in Fig. Q3-1, for **8 clock pulses**.

[5 marks]

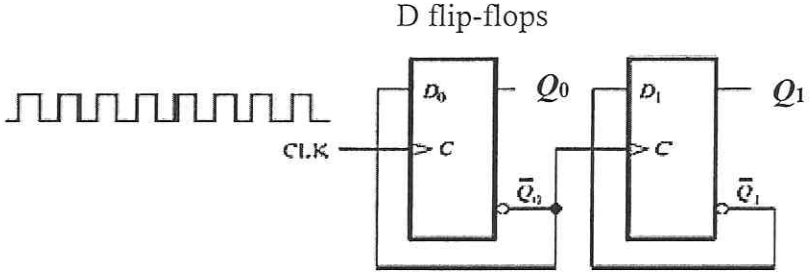


Fig. Q3-1

(b) Draw the Q output waveform of each of the following flip-flops when their inputs are as given in Fig. Q3-2 (page 5). Assume that Q is 0 initially. Reproduce Fig. Q3-2 in the answer booklet or tear and attach page 5 to the answer booklet.

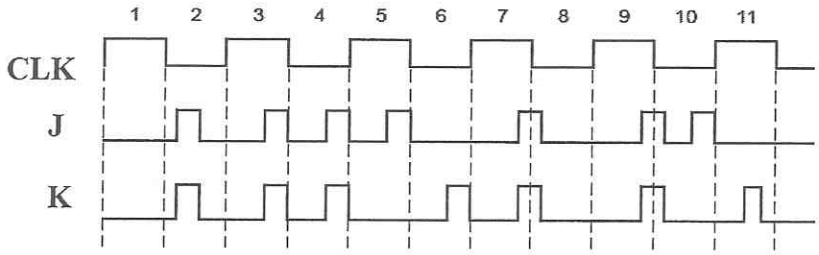
(i) Positive edge-triggered JK flip-flop

[3 marks]

(ii) Negative edge-triggered JK flip-flop

[3 marks]

Continued ...



Positive edge-triggered
(i) **Q**

Negative edge-triggered
(ii) **Q**

Fig. Q3-2

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Question 3 (continued)

(c) Answer the following questions about the design of a synchronous counter utilizing T flip-flops. The state diagram is as shown in Fig. Q3-3.

(i) Draw the excitation table of a T flip-flop.

[1 mark]

(ii) Draw the excitation table of the synchronous counter.

[4 marks]

(iii) With the aid of Karnaugh maps, simplify the logic expressions for the inputs of the flip-flops used in the synchronous counter. Show the worked Karnaugh maps.

[6 marks]

(iv) Draw the design of the counter using T flip-flops and logic gates.

[3 marks]

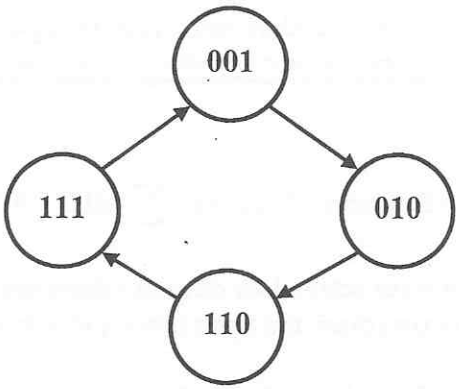

Fig. Q3-3

Continued ...

Question 4 (25 marks)

(a) Draw the **truth table** of 1-bit full adder.

[3 marks]

(b) Write down the **logic realization** (simplified Boolean expressions) of 1-bit full adder.

[3 marks]

(c) With the aid of a schematic diagram (please draw), **suggest a way** to connect 10 relays with binary input to one output port, such that each relay can be triggered individually via the output port. Use arrows to show the directions of signal flow.

[5 marks]

(d) With the aid of a schematic diagram (please draw), **suggest a way** to make a 4-to-16 decoder using 2-to-4 decoders with enable input. Label and number the inputs and outputs of the decoders (including the resultant 4-to-16 decoder).

[5 marks]

(e) **Implement** switching function $f(x, y, z) = \sum m(1,2,3,4,5,6)$ using each of the following:

(i) 3-to-8 decoder with active low outputs (draw the schematic diagram)
(ii) 4-to-1 multiplexer (draw the truth table and schematic diagram)

Let x be the most significant bit and z be the least significant bit.

[9 marks]

End of Paper